WHAT IS CLAIMED IS:

1. A process for fabricating a contact in a semiconductor substrate having a contact opening formed therein, comprising:

depositing a barrier layer in said contact opening and on at least a portion of said semiconductor substrate;

depositing a contact metal on said barrier layer within said contact opening;

removing a substantial portion of said contact metal and said barrier layer from said semiconductor substrate and forming a contact plug within said contact opening;

subjecting said contact plug to a temperature sufficient to anneal said barrier layer.

2. The process of Claim 1 wherein said depositing said barrier layer includes depositing a titanium layer and depositing a titanium nitride layer on said titanium layer.

3. The process of Claim 2 wherein said depositing includes depositing said titanium layer and said titanium nitride layer by physical vapor deposition.

4. The process of Claim 1 wherein said depositing said

barrier layer includes depositing said barrier layer in said contact opening formed in a dielectric and having an aspect ratio ranging from about 3:1 to about 5:1.

5. The process of Claim 1 wherein said depositing a contact metal includes depositing tungsten.

6. The process of Claim 5 wherein said depositing includes depositing said tungsten by chemical vapor deposition.

7. The process of Claim 1 wherein said subjecting includes subjecting said contact plug to a rapid thermal anneal process.

8. The process of Claim 1 wherein said depositing a barrier layer includes forming a thickness of said barrier layer ranging from about 5 nm to about 20 nm within said contact opening and forming a field area thickness of said barrier layer on said semiconductor substrate of about 75 nm or greater.

9. The process of Claim 8 wherein said thickness of said barrier layer within said contact opening is about 5% to about 20% of said field area thickness.

10. The process of Claim 8 wherein removing a substantial portion includes removing said contact metal and said barrier layer from said field area thickness.

11. The process of Claim 10 wherein said removing said contact metal and said barrier layer includes removing said contact metal and said barrier layer by chemical/mechanical polishing processes.

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12. A process for fabricating an integrated circuit, comprising:

forming an active device on a semiconductor substrate;

forming a contact opening in a dielectric deposited on said active device, said contact opening in electrical contact with said active device;

depositing a barrier layer in said contact opening and on at least a portion of said semiconductor substrate;

depositing a contact metal on said barrier layer within said contact opening;

removing a substantial portion of said contact metal and said barrier layer from said semiconductor substrate and forming a contact plug within said contact opening;

subjecting said contact plug to a temperature sufficient to anneal said barrier layer.

13. The process of Claim 12 wherein said depositing said barrier layer includes depositing a titanium layer and depositing a titanium nitride layer on said titanium layer.

14. The process of Claim 13 wherein said depositing includes depositing said titanium layer and said titanium nitride layer by physical vapor deposition.

15. The process of Claim 12 wherein said forming said contact opening includes forming said contact opening having an aspect ratio ranging from about 3:1 to about 5:1.

16. The process of Claim 12 wherein said depositing a contact metal includes depositing tungsten.

17. The process of Claim 16 wherein said depositing includes depositing said tungsten by chemical vapor deposition.

18. The process of Claim 12 wherein said subjecting includes subjecting said contact plug to a rapid thermal anneal process for a period ranging from about 5 seconds to about 60 seconds, a temperature of said rapid thermal anneal process ranging from about 600°C to about 750°C.

19. The process of Claim 12 wherein said depositing a barrier layer includes forming a thickness of said barrier layer ranging from about 5 nm to about 20 nm within said contact opening and forming a field area thickness of said barrier layer on said semiconductor substrate of about 75 nm or greater.

20. The process of Claim 19 wherein said thickness of said barrier layer within said contact opening is about 5% to about 20% of said field area thickness.

21. The process of Claim 19 wherein removing a substantial portion includes removing said contact metal and said barrier layer from said field area thickness.

22. The process of Claim 21 wherein said removing said contact metal and said barrier layer includes removing said contact metal and said barrier layer by chemical/mechanical polishing processes.

23. The process of Claim 12 wherein forming said active device includes forming an active device having a design width of about 0.25 microns or less.

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